```
RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940;  selected revisions: 3
description:
top level BOM
----------------------------
revision 3.937
date: 1995/07/27 05:29:21;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

Latest route result (48 disconnects, 48 timing paths) plus trivial Makefile
change and euterpe.status update
----------------------------
revision 3.936
date: 1995/07/26 18:47:55;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/tools

stgen: better init sequence to ensure similar reg commit counts between SW and
HW simulators
----------------------------
revision 3.935
date: 1995/07/22 23:29:50;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

correct heuristic for net ordering.  Latest route results
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/BOM,v
Working file: compass/BOM
head: 7.21
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 67;    selected revisions: 2
description:
----------------------------
revision 5.0
date: 1995/07/23 00:14:44;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe

The id chip is being used by tbr.
Ready to try snapshot build from the top again
----------------------------
revision 4.4
date: 1995/07/23 00:14:33;  author: chip;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/BOM,v
Working file: compass/layouts/BOM
```

```
head: 27.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 79;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 19.0
date: 1995/07/23 00:14:10;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe

The id chip is being used by tbr.
Ready to try snapshot build from the top again
----------------------------
revision 18.4
date: 1995/07/23 00:13:58;  author: chip;  state: Exp;  lines: +1 -10
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/BOM,v
Working file: doc/BOM
head: 22.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 70;    selected revisions: 2
description:
BOM for doc
----------------------------
revision 21.0
date: 1995/07/23 00:16:11;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe

The id chip is being used by tbr.
Ready to try snapshot build from the top again
----------------------------
revision 20.6
date: 1995/07/23 00:16:00;  author: chip;  state: Exp;  lines: +2 -5
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file:
/s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/allegro/rnd_probe6.brd,v
Working file: msts/DUT_boards/p620_00025_0000/allegro/rnd_probe6.brd
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 1.1
date: 1995/07/27 18:10:56;  author: pmayer;  state: Exp;
```

```
initial PCB layout
=============================================================================

RCS file: /s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/Makefile,v
Working file: msts/DUT_boards/p620_00025_0000/ged/Makefile
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.1
date: 1995/07/27 18:04:34;  author: pmayer;  state: Exp;
initial files for concept
=============================================================================

RCS file: /s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/Makefile.bck,v
Working file: msts/DUT_boards/p620_00025_0000/ged/Makefile.bck
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 1.1
date: 1995/07/27 18:04:36;  author: pmayer;  state: Exp;
initial files for concept
=============================================================================

RCS file:
/s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/Attic/Makefile.pkg,v
Working file: msts/DUT_boards/p620_00025_0000/ged/Makefile.pkg
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 1.1
date: 1995/07/27 18:04:38;  author: pmayer;  state: Exp;
initial files for concept
=============================================================================

RCS file: /s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/README,v
Working file: msts/DUT_boards/p620_00025_0000/ged/README
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
```

```
description:
----------------------------
revision 1.1
date: 1995/07/27 18:04:41;  author: pmayer;  state: Exp;
initial files for concept
=============================================================================

RCS file:
/s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/Attic/depend.pkg,v
Working file: msts/DUT_boards/p620_00025_0000/ged/depend.pkg
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 1.1
date: 1995/07/27 18:04:44;  author: pmayer;  state: Exp;
initial files for concept
=============================================================================

RCS file:
/s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/Attic/master.local,v
Working file: msts/DUT_boards/p620_00025_0000/ged/master.local
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 1.1
date: 1995/07/27 18:04:46;  author: pmayer;  state: Exp;
initial files for concept
=============================================================================

RCS file:
/s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/Attic/masterlogic.local,
v
Working file: msts/DUT_boards/p620_00025_0000/ged/masterlogic.local
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 1.1
date: 1995/07/27 18:04:48;  author: pmayer;  state: Exp;
initial files for concept
=============================================================================
```

```
RCS file:
/s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/Attic/startup.concept,v
Working file: msts/DUT_boards/p620_00025_0000/ged/startup.concept
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 1.1
date: 1995/07/27 18:04:49;  author: pmayer;  state: Exp;
initial files for concept
=============================================================================

RCS file:
/s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/probes/Attic/probes.lib,
v
Working file: msts/DUT_boards/p620_00025_0000/ged/probes/probes.lib
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 1.1
date: 1995/07/27 18:06:04;  author: pmayer;  state: Exp;
initial files for concept browser
=============================================================================

RCS file:
/s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/probes/Attic/probeslogic
.lib,v
Working file: msts/DUT_boards/p620_00025_0000/ged/probes/probeslogic.lib
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 1.1
date: 1995/07/27 18:06:06;  author: pmayer;  state: Exp;
initial files for concept browser
=============================================================================

RCS file:
/s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/probes/euterpe_mms_probe
/spice.1.1,v
Working file:
msts/DUT_boards/p620_00025_0000/ged/probes/euterpe_mms_probe/spice.1.1
head: 1.7
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 1.1
date: 1995/07/27 18:07:56;  author: pmayer;  state: Exp;
sheets for Euterpe_mms_probe Round DUT
=============================================================================

RCS file:
/s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/probes/euterpe_mms_probe
/spice.1.2,v
Working file:
msts/DUT_boards/p620_00025_0000/ged/probes/euterpe_mms_probe/spice.1.2
head: 1.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 1.1
date: 1995/07/27 18:07:58;  author: pmayer;  state: Exp;
sheets for Euterpe_mms_probe Round DUT
=============================================================================

RCS file:
/s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/probes/euterpe_mms_probe
/spice_cn.1.1,v
Working file:
msts/DUT_boards/p620_00025_0000/ged/probes/euterpe_mms_probe/spice_cn.1.1
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 1.1
date: 1995/07/27 18:08:00;  author: pmayer;  state: Exp;
sheets for Euterpe_mms_probe Round DUT
=============================================================================

RCS file:
/s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/probes/euterpe_mms_probe
/spice_cn.1.2,v
Working file:
msts/DUT_boards/p620_00025_0000/ged/probes/euterpe_mms_probe/spice_cn.1.2
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 1.1
date: 1995/07/27 18:08:03;  author: pmayer;  state: Exp;
sheets for Euterpe_mms_probe Round DUT
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;   selected revisions: 1
description:
----------------------------
revision 4.203
date: 1995/07/26 18:47:29;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/tools

stgen: better init sequence to ensure similar reg commit counts between SW and
HW simulators
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/status,v
Working file: verify/status
head: 3.64
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 64;    selected revisions: 2
description:
----------------------------
revision 3.36
date: 1995/07/28 03:02:59;  author: dit00;  state: Exp;  lines: +69 -0
Periodic update
----------------------------
revision 3.35
date: 1995/07/23 03:00:24;  author: dit00;  state: Exp;  lines: +49 -0
Periodic update
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/include/cerberus.h,v
Working file: verify/include/cerberus.h
head: 10.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 24;    selected revisions: 2
description:
----------------------------
revision 10.21
date: 1995/07/27 17:14:57;  author: jeffm;  state: Exp;  lines: +31 -1
```

```
Added turnoff_hermes macros.

Changed nbcheck to use cerberus address, rather than ltlb address -
so the loads would not complete during the timing run.
----------------------------
revision 10.20
date: 1995/07/25 18:07:45;  author: jeffm;  state: Exp;  lines: +11 -1
Add read/write of cerberus register 24.

Add regcheck and nbcheck subroutines. To check for nb shrink and leftover
register dependencies.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/include/end.S,v
Working file: verify/include/end.S
head: 1.38
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 38;    selected revisions: 3
description:
----------------------------
revision 1.38
date: 1995/07/27 21:28:50;  author: jeffm;  state: Exp;  lines: +2 -2
Bump up the time in nbcheck - there are two page crossers possible in the check
sequence
----------------------------
revision 1.37
date: 1995/07/27 17:14:59;  author: jeffm;  state: Exp;  lines: +3 -3
Added turnoff_hermes macros.

Changed nbcheck to use cerberus address, rather than ltlb address -
so the loads would not complete during the timing run.
----------------------------
revision 1.36
date: 1995/07/25 18:07:47;  author: jeffm;  state: Exp;  lines: +113 -1
Add read/write of cerberus register 24.

Add regcheck and nbcheck subroutines. To check for nb shrink and leftover
register dependencies.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/include/physaddr.h,v
Working file: verify/include/physaddr.h
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 24;    selected revisions: 1
description:
----------------------------
revision 4.24
date: 1995/07/27 00:20:16;  author: jeffm;  state: Exp;  lines: +4 -2
Getting it uptodate.
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verify/nasty/Makefile,v
Working file: verify/nasty/Makefile
head: 1.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 3
description:
----------------------------
revision 1.14
date: 1995/07/25 21:52:00;  author: jeffm;  state: Exp;  lines: +2 -2
Do lotsa stuff - cached stuff from hermes and dram, exceptions, interrupts,
uncached activity.
----------------------------
revision 1.13
date: 1995/07/25 18:17:00;  author: jeffm;  state: Exp;  lines: +5 -4
Oops. all0 target should not have been the default.
----------------------------
revision 1.12
date: 1995/07/25 18:10:45;  author: jeffm;  state: Exp;  lines: +4 -1
Made all0 target in Makefile.

Added regcheck and nbcheck to end of all the nasty tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty.S,v
Working file: verify/nasty/cachenasty.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/07/25 18:10:47;  author: jeffm;  state: Exp;  lines: +8 -5
Made all0 target in Makefile.

Added regcheck and nbcheck to end of all the nasty tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty2.S,v
Working file: verify/nasty/cachenasty2.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/07/25 18:10:50;  author: jeffm;  state: Exp;  lines: +6 -5
Made all0 target in Makefile.
```

```
Added regcheck and nbcheck to end of all the nasty tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty3.S,v
Working file: verify/nasty/cachenasty3.S
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/07/25 18:10:52;  author: jeffm;  state: Exp;  lines: +9 -7
Made all0 target in Makefile.

Added regcheck and nbcheck to end of all the nasty tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty4.S,v
Working file: verify/nasty/cachenasty4.S
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/07/25 18:10:54;  author: jeffm;  state: Exp;  lines: +7 -7
Made all0 target in Makefile.

Added regcheck and nbcheck to end of all the nasty tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty5.S,v
Working file: verify/nasty/cachenasty5.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 1.6
date: 1995/07/25 18:10:55;  author: jeffm;  state: Exp;  lines: +7 -7
Made all0 target in Makefile.

Added regcheck and nbcheck to end of all the nasty tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/cachesynchnasty.S,v
Working file: verify/nasty/cachesynchnasty.S
```

```
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/07/25 18:10:57;  author: jeffm;  state: Exp;  lines: +7 -6
Made all0 target in Makefile.

Added regcheck and nbcheck to end of all the nasty tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/cachesynchnasty2.S,v
Working file: verify/nasty/cachesynchnasty2.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 1.7
date: 1995/07/25 18:10:59;  author: jeffm;  state: Exp;  lines: +5 -5
Made all0 target in Makefile.

Added regcheck and nbcheck to end of all the nasty tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/exintbash.S,v
Working file: verify/nasty/exintbash.S
head: 3.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 3.5
date: 1995/07/25 18:11:01;  author: jeffm;  state: Exp;  lines: +8 -7
Made all0 target in Makefile.

Added regcheck and nbcheck to end of all the nasty tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/hermnasty.S,v
Working file: verify/nasty/hermnasty.S
head: 1.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
```

```
description:
----------------------------
revision 1.14
date: 1995/07/25 18:11:03;  author: jeffm;  state: Exp;  lines: +7 -3
Made all0 target in Makefile.

Added regcheck and nbcheck to end of all the nasty tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/nbcachebash.S,v
Working file: verify/nasty/nbcachebash.S
head: 18.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 18.1
date: 1995/07/25 21:51:57;  author: jeffm;  state: Exp;
Do lotsa stuff - cached stuff from hermes and dram, exceptions, interrupts,
uncached activity.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v
Working file: verify/obj/processor/inst/Makefile
head: 1.182
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 2
description:
----------------------------
revision 1.181
date: 1995/07/25 20:02:26;  author: jeffm;  state: Exp;  lines: +2 -2
Test machine check caused by cerberus error response.
----------------------------
revision 1.180
date: 1995/07/25 18:05:37;  author: jeffm;  state: Exp;  lines: +2 -2
New test - make sure that an icache hit, but with gtlb caching control
set to uncached physical, does not use the icache. Fails on terp - suspected
terp problem.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/obj/system/nasty/Makefile,v
Working file: verify/obj/system/nasty/Makefile
head: 1.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 3
description:
----------------------------
revision 1.14
```

```
date: 1995/07/25 21:52:00;  author: jeffm;  state: Exp;  lines: +2 -2
Do lotsa stuff - cached stuff from hermes and dram, exceptions, interrupts,
uncached activity.
----------------------------
revision 1.13
date: 1995/07/25 18:17:00;  author: jeffm;  state: Exp;  lines: +5 -4
Oops. all0 target should not have been the default.
----------------------------
revision 1.12
date: 1995/07/25 18:10:45;  author: jeffm;  state: Exp;  lines: +4 -1
Made all0 target in Makefile.

Added regcheck and nbcheck to end of all the nasty tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/icache_perf.S,v
Working file: verify/perf/icache_perf.S
head: 3.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
initial revision
----------------------------
revision 3.1
date: 1995/07/26 21:19:08;  author: claseman;  state: Exp;
initial revision
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/icachemiss_perf.S,v
Working file: verify/perf/icachemiss_perf.S
head: 1.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 1.5
date: 1995/07/26 21:18:48;  author: claseman;  state: Exp;  lines: +12 -89
fix interrupt problem
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/BOM,v
Working file: verify/random/BOM
head: 8.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 1
description:
releasebom adding BOM
----------------------------
```

```
revision 5.0
date: 1995/07/23 00:20:50;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe

The id chip is being used by tbr.
Ready to try snapshot build from the top again
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2695.S,v
Working file: verify/random/regdepend_r2695.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/25 17:06:34;  author: dit00;  state: Exp;  lines: +4 -0
Add compare register commit end signal
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r3064.S,v
Working file: verify/random/regdepend_r3064.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/25 17:06:31;  author: dit00;  state: Exp;  lines: +4 -0
Add compare register commit end signal
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r3561.S,v
Working file: verify/random/regdepend_r3561.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/25 17:06:28;  author: dit00;  state: Exp;  lines: +4 -0
Add compare register commit end signal
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r3957.S,v
Working file: verify/random/regdepend_r3957.S
head: 3.2
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/24 15:33:51;  author: dit00;  state: Exp;  lines: +4 -0
Add register commit compare done indication
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r4157.S,v
Working file: verify/random/regdepend_r4157.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/24 15:33:55;  author: dit00;  state: Exp;  lines: +4 -0
Add register commit compare done indication
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r4356.S,v
Working file: verify/random/regdepend_r4356.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/24 15:33:58;  author: dit00;  state: Exp;  lines: +4 -0
Add register commit compare done indication
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r4552.S,v
Working file: verify/random/regdepend_r4552.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/24 15:34:00;  author: dit00;  state: Exp;  lines: +4 -0
Add register commit compare done indication
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r4752.S,v
```

```
Working file: verify/random/regdepend_r4752.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/24 15:34:04;  author: dit00;  state: Exp;  lines: +4 -0
Add register commit compare done indication
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r4951.S,v
Working file: verify/random/regdepend_r4951.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/26 14:22:54;  author: dit00;  state: Exp;  lines: +4 -0
Add compare register commit end code
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r5152.S,v
Working file: verify/random/regdepend_r5152.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/26 14:22:57;  author: dit00;  state: Exp;  lines: +4 -0
Add compare register commit end code
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r5352.S,v
Working file: verify/random/regdepend_r5352.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/26 14:23:00;  author: dit00;  state: Exp;  lines: +4 -0
Add compare register commit end code
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r6152.S,v
Working file: verify/random/regdepend_r6152.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/25 17:06:25;  author: dit00;  state: Exp;  lines: +3 -0
Add compare register commit end signal
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r6352.S,v
Working file: verify/random/regdepend_r6352.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/25 17:06:21;  author: dit00;  state: Exp;  lines: +3 -0
Add compare register commit end signal
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r6552.S,v
Working file: verify/random/regdepend_r6552.S
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/07/25 17:06:18;  author: dit00;  state: Exp;  lines: +3 -0
Add compare register commit end signal
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r7563.S,v
Working file: verify/random/regdepend_r7563.S
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
```

```
revision 4.2
date: 1995/07/25 17:06:13;  author: dit00;  state: Exp;  lines: +3 -0
Add compare register commit end signal
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r7763.S,v
Working file: verify/random/regdepend_r7763.S
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/07/25 17:06:10;  author: dit00;  state: Exp;  lines: +3 -0
Add compare register commit end signal
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r7963.S,v
Working file: verify/random/regdepend_r7963.S
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/07/25 17:06:06;  author: dit00;  state: Exp;  lines: +3 -0
Add compare register commit end signal
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r8558.S,v
Working file: verify/random/regdepend_r8558.S
head: 4.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 4.1
date: 1995/07/25 17:06:01;  author: dit00;  state: Exp;
Add compare register commit end signal
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r8778.S,v
Working file: verify/random/regdepend_r8778.S
head: 4.1
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 4.1
date: 1995/07/25 17:05:58;  author: dit00;  state: Exp;
Add compare register commit end signal
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r8985.S,v
Working file: verify/random/regdepend_r8985.S
head: 4.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 4.1
date: 1995/07/25 17:05:56;  author: dit00;  state: Exp;
Add compare register commit end signal
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r9180.S,v
Working file: verify/random/regdepend_r9180.S
head: 4.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 4.1
date: 1995/07/25 17:05:53;  author: dit00;  state: Exp;
Add compare register commit end signal
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r9380.S,v
Working file: verify/random/regdepend_r9380.S
head: 4.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 4.1
date: 1995/07/25 17:05:50;  author: dit00;  state: Exp;
Add compare register commit end signal
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/status,v
Working file: verify/random/status
head: 2.26
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 2
description:
----------------------------
revision 2.19
date: 1995/07/28 03:05:06;  author: dit00;  state: Exp;  lines: +4 -0
Periodic update
----------------------------
revision 2.18
date: 1995/07/26 14:24:13;  author: dit00;  state: Exp;  lines: +17 -0
Periodic update
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r10803.S,v
Working file: verify/random/stgen_r10803.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/25 17:30:24;  author: dit00;  state: Exp;  lines: +26 -1
Add compare register commit end signal and cyl stall code
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r10987.S,v
Working file: verify/random/stgen_r10987.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/25 17:30:28;  author: dit00;  state: Exp;  lines: +26 -1
Add compare register commit end signal and cyl stall code
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r11362.S,v
Working file: verify/random/stgen_r11362.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/25 17:30:32;  author: dit00;  state: Exp;  lines: +25 -0
```

```
Add compare register commit end signal and cyl stall code
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r11544.S,v
Working file: verify/random/stgen_r11544.S
head: 4.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/07/25 17:30:37;  author: dit00;  state: Exp;  lines: +25 -0
Add compare register commit end signal and cyl stall code
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r8191.S,v
Working file: verify/random/stgen_r8191.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/25 17:30:21;  author: dit00;  state: Exp;  lines: +26 -1
Add compare register commit end signal and cyl stall code
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/template,v
Working file: verify/random/template
head: 2.33
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 33;    selected revisions: 2
description:
----------------------------
revision 2.23
date: 1995/07/28 03:05:04;  author: dit00;  state: Exp;  lines: +8 -7
Periodic update
----------------------------
revision 2.22
date: 1995/07/26 14:24:14;  author: dit00;  state: Exp;  lines: +102 -101
Periodic update
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/BOM,v
Working file: verify/standalone/BOM
head: 6.0
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 85;    selected revisions: 2
description:
----------------------------
revision 5.0
date: 1995/07/23 00:30:14;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe

The id chip is being used by tbr.
Ready to try snapshot build from the top again
----------------------------
revision 4.36
date: 1995/07/23 00:30:02;  author: chip;  state: Exp;  lines: +5 -17
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/BOM,v
Working file: verify/tools/BOM
head: 13.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 90;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 12.0
date: 1995/07/26 18:47:16;  author: doi;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/tools

stgen: better init sequence to ensure similar reg commit counts between SW and
HW simulators
----------------------------
revision 11.1
date: 1995/07/26 18:47:09;  author: doi;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/stgen,v
Working file: verify/tools/stgen
head: 5.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 5.12
date: 1995/07/26 18:43:03;  author: doi;  state: Exp;  lines: +51 -10
There were problems with my last changes.  Any type of synchronization
step will introduce differences between the register commits that the
software and hardware simulators report.  As a result the test has
been modified to introduce a dead-reckoned time delay for all cylinders
but zero (if a delay is indeed required).
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v
Working file: verify/toplevel/Makefile
head: 1.185
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 185;   selected revisions: 4
description:
----------------------------
revision 1.183
date: 1995/07/27 16:51:22;  author: lisar;  state: Exp;  lines: +2 -2
Corrected spelling error in Ibash test name
----------------------------
revision 1.182
date: 1995/07/27 16:46:33;  author: lisar;  state: Exp;  lines: +11 -3
Added Ibash variations
----------------------------
revision 1.181
date: 1995/07/25 20:02:26;  author: jeffm;  state: Exp;  lines: +2 -2
Test machine check caused by cerberus error response.
----------------------------
revision 1.180
date: 1995/07/25 18:05:37;  author: jeffm;  state: Exp;  lines: +2 -2
New test - make sure that an icache hit, but with gtlb caching control
set to uncached physical, does not use the icache. Fails on terp - suspected
terp problem.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/cerberrresp.S,v
Working file: verify/toplevel/cerberrresp.S
head: 41.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 41.1
date: 1995/07/25 20:02:23;  author: jeffm;  state: Exp;
Test machine check caused by cerberus error response.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/eu.in,v
Working file: verify/toplevel/eu.in
head: 2.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 2.4
```

```
date: 1995/07/27 17:55:40;  author: lisar;  state: Exp;  lines: +1 -1
Wait a really long time instead of just a long time
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes_Ibash_nd_stomp.hconfig,v
Working file: verify/toplevel/hermes_Ibash_nd_stomp.hconfig
head: 41.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 41.1
date: 1995/07/27 16:50:30;  author: lisar;  state: Exp;
For the Ibash variations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes_Ibash_nodelay.hconfig,v
Working file: verify/toplevel/hermes_Ibash_nodelay.hconfig
head: 41.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 41.1
date: 1995/07/27 16:50:31;  author: lisar;  state: Exp;
For the Ibash variations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes_Ibash_stomp.hconfig,v
Working file: verify/toplevel/hermes_Ibash_stomp.hconfig
head: 41.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 41.1
date: 1995/07/27 16:50:28;  author: lisar;  state: Exp;
For the Ibash variations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermesnatest.S,v
Working file: verify/toplevel/hermesnatest.S
head: 41.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
```

```
description:
----------------------------
revision 41.2
date: 1995/07/27 00:19:12;  author: jeffm;  state: Exp;  lines: +4 -6
To get this uptodate before moving it.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/icachetransim.S,v
Working file: verify/toplevel/icachetransim.S
head: 41.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 41.2
date: 1995/07/28 00:45:10;  author: jeffm;  state: Exp;  lines: +9 -9
Fixed use of uninit. register.
----------------------------
revision 41.1
date: 1995/07/25 18:05:40;  author: jeffm;  state: Exp;
New test - make sure that an icache hit, but with gtlb caching control
set to uncached physical, does not use the icache. Fails on terp - suspected
terp problem.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/template,v
Working file: verify/toplevel/template
head: 1.148
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;   selected revisions: 1
description:
----------------------------
revision 1.127
date: 1995/07/28 03:03:38;  author: dit00;  state: Exp;  lines: +10 -7
Periodic update
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390;  selected revisions: 2
description:
top level verilog BOM
----------------------------
revision 4.12
date: 1995/07/27 05:29:03;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc
```

```
Latest route result (48 disconnects, 48 timing paths) plus trivial Makefile
change and euterpe.status update
----------------------------
revision 4.11
date: 1995/07/22 23:29:28;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

correct heuristic for net ordering.  Latest route results
============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/Makefile,v
Working file: verilog/Makefile
head: 1.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
Makefile
----------------------------
revision 1.8
date: 1995/07/23 16:37:22;  author: chip;  state: Exp;  lines: +3 -3
Stop Makefile arbitrarily writing log to makerrs
============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737;  selected revisions: 4
description:
----------------------------
revision 338.0
date: 1995/07/27 05:28:40;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

Latest route result (48 disconnects, 48 timing paths) plus trivial Makefile
change and euterpe.status update
----------------------------
revision 337.1
date: 1995/07/27 05:28:25;  author: tbr;  state: Exp;  lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 337.0
date: 1995/07/22 23:29:05;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

correct heuristic for net ordering.  Latest route results
----------------------------
revision 336.1
date: 1995/07/22 23:28:51;  author: tbr;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile,v
Working file: verilog/bsrc/Makefile
head: 1.255
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 255;   selected revisions: 1
description:
----------------------------
revision 1.251
date: 1995/07/27 00:16:02;  author: lisar;  state: Exp;  lines: +7 -4
Added explicit rule to create .xp_dir/.xp_dir independant of whether .xp_dir
exists
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v
Working file: verilog/bsrc/Makefile.tst
head: 40.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;   selected revisions: 3
description:
----------------------------
revision 40.98
date: 1995/07/22 22:58:53;  author: tbr;  state: Exp;  lines: +8 -8
oops, short net ordering had same problem
----------------------------
revision 40.97
date: 1995/07/22 22:50:12;  author: tbr;  state: Exp;  lines: +8 -8
correct all.net ordering script
----------------------------
revision 40.96
date: 1995/07/22 20:15:59;  author: tbr;  state: Exp;  lines: +9 -7
make TOPT_ONLYUP the default
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.netcap,v
Working file: verilog/bsrc/chip_euterpe-base.netcap
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 2
description:
----------------------------
revision 312.18
date: 1995/07/27 04:59:33;  author: tbr;  state: Exp;  lines: +29023 -29038
latest route result
----------------------------
revision 312.17
date: 1995/07/22 22:55:19;  author: tbr;  state: Exp;  lines: +28301 -28302
```

```
another iteration
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.pim,v
Working file: verilog/bsrc/chip_euterpe-base.pim
head: 312.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23;    selected revisions: 2
description:
----------------------------
revision 312.19
date: 1995/07/27 04:54:44;  author: tbr;  state: Exp;  lines: +7 -7
latest route result
----------------------------
revision 312.18
date: 1995/07/22 23:00:46;  author: tbr;  state: Exp;  lines: +1 -1
another iteration
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.strength,v
Working file: verilog/bsrc/chip_euterpe-base.strength
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 2
description:
----------------------------
revision 312.18
date: 1995/07/27 05:04:13;  author: tbr;  state: Exp;  lines: +309 -309
latest route result
----------------------------
revision 312.17
date: 1995/07/22 22:59:42;  author: tbr;  state: Exp;  lines: +152 -152
another iteration
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.status,v
Working file: verilog/bsrc/euterpe.status
head: 24.83
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 83;    selected revisions: 1
description:
----------------------------
revision 24.76
date: 1995/07/25 18:59:31;  author: jeffm;  state: Exp;  lines: +5 -1
Document that the cerberus master does not check for reserved transaction
codes or inconsistant payload lenths in responses, and that the cerberus
slave does not check for consistancy in payload lengths and transactions that
are directed to it.
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/i_h_euterpe_wrap.tb,v
Working file: verilog/bsrc/i_h_euterpe_wrap.tb
head: 325.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 325.4
date: 1995/07/27 19:00:47;  author: lisar;  state: Exp;  lines: +3 -2
Just use hconfig
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu_control.pim,v
Working file: verilog/bsrc/uu/uu_control.pim
head: 68.60
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 60;    selected revisions: 1
description:
----------------------------
revision 68.60
date: 1995/07/27 06:20:37;  author: dickson;  state: Exp;  lines: +6 -7
timing fix for nb to uu paths.
=============================================================================
```